

WE CLAIM:

1. A system for modeling a package assembly for an integrated circuit device [electronic structure], comprising:

- 5 an input data generator operable to generate input data comprising information describing a plurality of characteristics of a package assembly [structure] to be modeled,
 wherein said plurality of characteristics comprise
10 a plurality of segments, subdivisions, and compositions;
 a segmentation generator, coupled to said input data generator, operable to select the most effective segments of said package, [structure to be modeled]
15 to organize the sequence of said segments, to store the data related to said sequenced segments into a segment file, and to convert said segment file into a format suitable for electrical analysis;
 an analysis generator, coupled to said segmentation generator, operable to electrically analyze said
20 converted segment file in a plurality of calculation programs, executed in sequence, and to create electrical analysis output files;
 an integrator, coupled to said analysis generator,
25 operable to integrate said analysis output files in controlled sequence into a single model file, to quantify alternative choices, and to store said file in a report storage; and
 an output generator, coupled to said integrator,
30 operable to create summary files in specific formats or displays.

2. The system according to Claim 1 wherein said segmentation generator comprises:

5 a segment selector, coupled to said input data generator, operable to select leadframe segments and test lines of said package [structure] to be modeled, select the input data correlated to said segments and test lines, and file said data in an input data storage;

10 a sequence organizer, coupled to said input data storage, operable to arrange said segments in the correct order for modeling and to create segment data files; and

15 a model data translator, coupled to said segment data file, operable to read said segment data files, to convert said segment into a format suitable for electrical analysis, and to create an analysis input storage, suitable for electrical analysis to be performed by a plurality of calculation programs executed in sequence.

20 3. The system according to Claim 2 further comprising a source of parametric data coupled to said sequence organizer.

Claims 4-8 cancelled.

25 9. The system according to claim 1 wherein said analysis generator comprises two-dimensional and three-dimensional electrical calculation means operable to cover all test lines and specified frequencies.

30 10. The system according to Claim 1 wherein said analysis generator produces a multitude of patterns comprising electrical resistances, capacitances, and inductances.

11. The system according to Claim 1 further comprising an integrator operable to calculate the scattering parameters for electrical high frequency assembly.

WE CLAIM:

1. A system for modeling a package assembly for an integrated circuit device, comprising:

- 5 an input data generator operable to generate input data comprising information describing a plurality of characteristics of a package assembly to be modeled,
 wherein said plurality of characteristics comprise
10 a plurality of segments, subdivisions, and compositions;
 a segmentation generator, coupled to said input data generator, operable to select the most effective segments of said package, to organize the sequence
15 of said segments, to store the data related to said sequenced segments into a segment file, and to convert said segment file into a format suitable for electrical analysis;
 an analysis generator, coupled to said segmentation generator, operable to electrically analyze said
20 converted segment file in a plurality of calculation programs, executed in sequence, and to create electrical analysis output files;
 an integrator, coupled to said analysis generator,
25 operable to integrate said analysis output files in controlled sequence into a single model file, to quantify alternative choices, and to store said file in a report storage; and
 an output generator, coupled to said integrator,
30 operable to create summary files in specific formats or displays.

2. The system according to Claim 1 wherein said segmentation generator comprises:

- a segment selector, coupled to said input data generator, operable to select leadframe segments and test lines of said package to be modeled, select the input data correlated to said segments and test lines, and file said data in an input data storage;
- a sequence organizer, coupled to said input data storage, operable to arrange said segments in the correct order for modeling and to create segment data files; and
- a model data translator, coupled to said segment data file, operable to read said segment data files, to convert said segment into a format suitable for electrical analysis, and to create an analysis input storage, suitable for electrical analysis to be performed by a plurality of calculation programs executed in sequence.
3. The system according to Claim 2 further comprising a source of parametric data coupled to said sequence organizer.
9. The system according to claim 1 wherein said analysis generator comprises two-dimensional and three-dimensional electrical calculation means operable to cover all test lines and specified frequencies.
10. The system according to Claim 1 wherein said analysis generator produces a multitude of patterns comprising electrical resistances, capacitances, and inductances.
11. The system according to Claim 1 further comprising an integrator operable to calculate the scattering parameters for electrical high frequency assembly.
12. A computer system for modeling an electronic structure, comprising:
an input data generator operable to accept and store

graphical, geometric, functional and compositional inputs and to create patterns of electrical conductors and insulators of the structure to be modeled;

5 a segment selector, coupled to said input data generator, operable to select segments and test lines of the structure to be modeled, to select the input data correlated to said segments and test lines from said data generator, and to create
10 input data files;

a user interface including an operations controller, coupled to said input data files, operable to respond to user commands for controlling execution and timing of a multitude of operations of said
15 computer system;

a sequence organizer, coupled to said input data file and further to additional parametric data storage, operable to arrange said segments in the correct order for modeling and to create segment data
20 files;

a model data translator, coupled to said segment data file and further to said operations controller, operable to read said segment data files, to follow instructions from said operations
25 controller, to convert said segment data into a format suitable for electrical analysis, and to store the results in an analysis input storage;

an analysis generator, coupled to said analysis input storage and further to said operations controller, operable to execute a plurality of electrical calculation programs in sequence and to create
30 electrical analysis output files;

a model data integrator, coupled to said analysis output files and further to said operations

controller, operable to integrate said analysis output files in controlled sequence into a single model file and to store said file in a report storage; and

5 an output generator, coupled to said model data integrator and further to said user interface, operable to create said model for each frequency analysis.

10 13. The computer system according to Claim 12 wherein said output generator creates said model in the format of SPICE-acceptable decks, summary and report files, IBIS decks, and displays.

15 14. The computer system according to Claim 12 further comprising a coupling of said parameter data storage to said user interface operable to transmit parametric data to said parameter data storage.

15. The computer system according to Claim 12 wherein said input data generator comprises:

20 an input unit operable to create patterns of electrical conductors and insulators;
 a graphical input unit operable to accept, select and read geometric and graphical programs; and
 a parametric input unit operable to accept compositional and functional parameters.

25 16. The computer system according to Claim 15 wherein said geometric and graphical programs are selected from a group consisting of pro/ENGINEER and AutoCAD programs.

30 17. The computer system according to Claim 12 wherein said input data files, coupled to said segment selector, comprise storage of the input data after segment and test line selection in a format suitable for the selected graphical input program.

18. The computer system according to Claim 17 wherein said input data storage is in the IGES format for input data

dimensional analysis; and
for each test line of said structure to be modeled
that traverses regions of different dielectric
constants, electrical potentials, geometries, or
5 symmetries.

22. A computer-implemented method for constructing a model
of an electronic structure, comprising the steps of:
generating input data comprising information
describing a plurality of characteristics of a
10 structure to be modeled, wherein said plurality
of characteristics comprise a plurality of
segments, subdivision, and compositions;
generating segments of said structure to be modeled,
selecting said segments, organizing the sequence
15 of said segments, storing the data related to
said sequenced segments into a segment file, and
converting said segment file into a format
suitable for electrical analysis;
electrically analyzing said converted segment file
20 in a plurality of calculation programs executed
in sequence, and creating electrical analysis
output files;
integrating said analysis output files in controlled
sequence into a single model file and storing
25 said file in a report storage; and
creating summary files in specific formats or
displays.

23. The computer-implemented method according to Claim 22
wherein said step of generating input data of said
30 electronic structure comprises:
creating patterns of electrical conductors and
insulators of said electronic structure;
accepting, selecting and reading geometric and
graphical programs describing a plurality of

characteristics of said electronic structure; and
accepting compositional and functional parameters of
said electronic structure.

24. The computer-implemented method according to Claim 22

5 wherein said step of generating segments comprises:

selecting segments and test lines of said structure
to be modeled, selecting the input data
correlated to said segments and test lines, and
filing said data in an input data storage;

10 arranging said segments in the correct order for
modeling, and creating a segment data storage;
and

converting said segment data storage into a format
suitable for electrical analysis, and creating an
15 analysis input storage suitable for electrical
analysis to be performed by a plurality of
programs executed in sequence.

25. The computer-implemented method according to Claim 24

20 wherein said step of converting said segment data
storage into a format suitable for electrical analysis
comprises:

reading the first segment from said segment data
storage;

identifying all element groups that form a segment

25 by a series of automatic steps comprising:

determining whether the end of the three-
dimensional segment has been reached;
finding the edges of the geometry in said
segment;

30 ordering said edges; and

determining whether the end of the two-
dimensional segment has been reached;

converting the three-dimensional segment data and
the two-dimensional segment data into the input

format for electrical analysis;
transferring the data in said input format to the
analysis input storage;
determining whether another segment is stored in
5 said segment data storage; and
repeating all said steps until all segments in said
segment data storage have been read and
converted.

26. The computer-implemented method according to Claim 22
10 wherein said step of integrating said analysis output
files into a single model file comprises:
 reading the analysis output as stored in said
 analysis output files;
 controlling said analysis output by reading each
15 segment from said segment data storage and
 collating a sequence list;
 determining electrical connectivity as based on
 symmetry and branching of said collated sequence
 list;
20 creating analysis output in a suitable format; and
 storing said analysis output in a report storage.

27. The computer-implemented method according to Claim 26
 wherein said collated sequence list, based on symmetry
 and branching, generates a model of a complete
25 electronic structure.

28. The computer-implemented method according to Claim 26
 wherein said format of the analysis output is the SPICE-
 model format.

29. The computer-implemented method according to Claim 26
30 wherein said analysis output has lumped or distributed
 format.

30. The computer-implemented method according to Claim 22
 further comprising the steps of :
 controlling process operations by responding to user

commands; and
automatically controlling execution and timing of a
plurality of operations.

31. The computer-implemented method according to Claim 30
5 wherein said step of controlling operations comprises
the steps of:

coordinating the sequence of the electrical analysis
calculation programs;

10 instructing the start of the execution of each said
calculation programs;

processing signals at the end of each program
execution;

controlling the successful completion of each said
calculation programs, thereby accepting
15 successful executions and refusing failed
executions;

searching for the next said segment in said sequence;

controlling the storage of the completed analysis
results in the analysis output files; and

20 instructing the advancement of said results to the
model data integrator.

32. A system as in claim 1 wherein said segment selector is
operable to define a set of continuous conductor subdivisions.

25 33. A system as in claim 32 wherein said sequence organizer
is operable to define said subdivisions starting from the chip
side of the package.